



Application Note
netX 5
Serial and Parallel Host Interface

Hilscher Gesellschaft für Systemautomation mbH

www.hilscher.com

DOC100204AN01EN | Revision 1 | English | 2010-02 | Released | Public

Table of Contents

1	Introduction.....	3
1.1	About this Document.....	3
1.2	List of Revisions	3
2	netX5 Read Access	4
2.1	Access Table.....	4
3	Appendix	6
3.1	List of Tables	6
3.2	Contacts	7

1 Introduction

1.1 About this Document

This manual describes which rules to take into account during data access using netX5 with either an 8-bit or a 16 bit host interface or with a serial host interface depending on whether the options INTRAM/INTLOGIC `byte_read` and xPEC RAM `byte_read` are enabled or disabled.

1.2 List of Revisions

Rev	Date	Name	Chapter	Revision
1	2010-02-02		all	Created

Table 1: List of Revisions

2 netX5 Read Access

2.1 Access Table

The following table explains which rules to take into account during data access with either an 8-bit or a 16 bit host interface or with a serial host interface depending on whether the options INTRAM/INTLOGIC `byte_read` and xPEC RAM `byte_read` are enabled or disabled.

The table shows which of the notes below has to be applied:

<i>8 Bit Host Interface</i> Access type	INTRAM/INTLOGIC	byte_read	xPEC RAM	byte_read
	enabled	disabled	enabled	disabled
byte	Note 2	Note 3	Note 4	Note 6
word	Note 1.1	Note 3	Note 5	Note 6
dword	Note 1.2	Note 2	Note 5	Note 4

<i>16 Bit Host Interface</i> Access type	INTRAM/INTLOGIC	byte_read	xPEC RAM	byte_read
	enabled	disabled	enabled	disabled
byte	Note 2	Note 3	Note 4	Note 6
word	Note 2	Note 3	Note 4	Note 6
dword	Note 1.1	Note 2	Note 5	Note 4

<i>serielles Host Interface</i> Access type	INTRAM/INTLOGIC	byte_read	xPEC RAM	byte_read
	enabled	disabled	enabled	disabled
byte	Note 9,10,13	Note 7	Note 9,11,13	Note 7
word	Note 7	Note 7	Note 7	Note 7
dword	Note 7	Note 8	Note 7	Note 8,12

Table 2: Access Table

Notes

- 1.1) Internally the host interface performs two accesses, the timing constraints of the host interface must be followed, because technically no Dummy Read SW can be inserted.
- 1.2) Internally the host interface performs four accesses, the timing constraints of the host interface must be followed, because technically no Dummy Read SW can be inserted.
- 2) When following with the timing constraints of the host interface, a Dummy Read can be omitted after every write access, otherwise performing a Dummy Read offers complete security.
- 3) No dummy reads are permitted as accesses would be deleted, the timing constraints of the host interface must be followed.
- 4) Dummy reads must be performed after every write access in order to insure correct completion of the write access.
- 5) Accesses are not possible as the xPEC may block its memory in a non-deterministic manner and the width of the write access exceeds the width of the host interface.
- 6) Accesses are not possible as the xPEC may block its memory in a non-deterministic manner and the internal width of the write access exceeds the width of the host interface

- 7) Only byte-wise access to the DPM areas with `ByteReadEn=1` is allowed respectively only dword access to DPM areas with `ByteReadEn=0` is allowed.
- 8) Send `hdr` with address plus always 4 data bytes, then put CS high again.
- 9) Send `hdr` with address plus always 1 data bytes, then put CS high again. dummy reads are not possible as the DPM Error detection on areas with `ByteRdEn=1` is erroneous.
- 10) Follow the host interface timing constraints
- 11) Follow the host interface timing constraints and take care of worst case times for xPEC RAM blockade by accesses of xPEC-ALU/XC DMA to its own memory.
- 12) Check DPM state after every access for failure in order to be able to repeat the access if necessary.
- 13) At reading, a complete dw is internally read from the netX5 and internally latched, all further read accesses do not cause further internal accesses to the netX as long as the subsequent read addresses are located within the same dw, i.e. for insuring the correctness of current data perform a Dummy Read onto another address (e.g. INTRAM, no DPM `CfgStat` access) after a completely finished access.

Note When using serial DPM the DPM_PIOs 31:12 may not be used by the host, because the ZPU cyclically accesses the register `dpm_pio_out1`.

3 Appendix

3.1 List of Tables

Table 1: List of Revisions	3
Table 2: Access Table.....	4

3.2 Contacts

Headquarters

Germany

Hilscher Gesellschaft für
Systemautomation mbH
Rheinstrasse 15
65795 Hattersheim
Phone: +49 (0) 6190 9907-0
Fax: +49 (0) 6190 9907-50
E-Mail: info@hilscher.com

Support

Phone: +49 (0) 6190 9907-99
E-Mail: de.support@hilscher.com

Subsidiaries

China

Hilscher Ges.f.Systemaut. mbH
Shanghai Representative Office
200010 Shanghai
Phone: +86 (0) 21-6355-5161
E-Mail: info@hilscher.cn

Support

Phone: +86 (0) 21-6355-5161
E-Mail: cn.support@hilscher.com

France

Hilscher France S.a.r.l.
69500 Bron
Phone: +33 (0) 4 72 37 98 40
E-Mail: info@hilscher.fr

Support

Phone: +33 (0) 4 72 37 98 40
E-Mail: fr.support@hilscher.com

India

Hilscher India Pvt. Ltd.
New Delhi - 110 025
Phone: +91 9810269248
E-Mail: info@hilscher.in

Italy

Hilscher Italia srl
20090 Vimodrone (MI)
Phone: +39 02 25007068
E-Mail: info@hilscher.it

Support

Phone: +39/02 25007068
E-Mail: it.support@hilscher.com

Japan

Hilscher Japan KK
Tokyo, 160-0022
Phone: +81 (0) 3-5362-0521
E-Mail: info@hilscher.jp

Support

Phone: +81 (0) 3-5362-0521
E-Mail: jp.support@hilscher.com

Korea

Hilscher Korea Inc.
Suwon-Si, 443-810
Phone: +82-31-204-6190
E-Mail: info@hilscher.kr

Switzerland

Hilscher Swiss GmbH
4500 Solothurn
Phone: +41 (0) 32 623 6633
E-Mail: info@hilscher.ch

Support

Phone: +49 (0) 6190 9907-99
E-Mail: ch.support@hilscher.com

USA

Hilscher North America, Inc.
Lisle, IL 60532
Phone: +1 630-505-5301
E-Mail: info@hilscher.us

Support

Phone: +1 630-505-5301
E-Mail: us.support@hilscher.com